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PATENT APPLICATION C. Will

NAK1-BQ83

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eiji Takahashi et al.

Serial No.: 10/029,571

Filed: December 20, 2001

For: MULTILAYER BOARD IN WHICH WIRING OF SIGNAL LINE THAT REQUIRES TAMPER-RESISTANCE IS COVERED BY COMPONENT OR FOIL, DESIGN APPARATUS, METHOD, AND PROGRAM FOR THE MULTILAYER BOARD, AND MEDIUM RECORDING THE PROGRAM

Examiner:

Group Art Unit: 2857

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February 11, 2002

#### INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

In compliance with the duty of disclosure as set forth in 37 C.F.R. § 1.56 and in conformance with 37 C.F.R. §§ 1.97(c) - 1.98, applicants wish to bring to the attention of the United States Patent Examiner the following references:

#### **U.S. PATENTS**

5,905,640

Hutchison et al.

### **FOREIGN PATENTS**

Japanese Patent No. 11145401A w/ English abstract

Copies of these references are enclosed herewith and are listed on the attached PTO Form 1449.



# **COPY OF PAPERS**

RECEIVED TO THE ROOM In the event an Office Action is mailed before the IDS is received by the Patent Office, please charge the fee of \$180.00 to Deposit Account No. 16-2462.

If the Examiner believes that a telephone interview would help further the prosecution of this case, he is respectfully requested to contact the undersigned attorney at the listed telephone number.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on February 11, 2002.

By: Marc Fregoso

Date: February 11, 2002

Respectfully submitted,

PRICE AND GESS

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